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Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Salman Akram, David R. Hembree

Serial No.: unk

Filed: July 27, 2001 (herewith)

For: Method of Forming A Test Insert For Interfacing A Device Containing Contact Bumps With A Test Substrate

Group Art Unit: unk

Examiner: unk

Atty. Dkt. No.: MCRO290--2/LWT

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Please consider this preliminary amendment. It is not believe that any fee is due in order for the Office to consider this response. However, should any fees be due, the Commissioner is authorized to deduct any necessary amounts from Deposit Account No. 01-2508/MCRO290--2/LWT.

I. AMENDMENTS

- **Please cancel claims 1-106.**

- **Please add the following new claims:**

107. (New) A method for making an insert for electrically interfacing an electronic device to a support substrate, the electronic device containing a plurality of contact bumps and a protrusion, the support substrate containing a plurality of conductive members, the insert having first and second sides, the method comprising:

(a) providing an insert substrate;

(b) forming in the first side of the insert substrate a plurality of pockets configured to receive and contact the contact bumps;

(c) forming in the first side of the insert substrate a recess configured to receive the protrusion when the contact bumps are received in the plurality of pockets;

(d) forming a dielectric material over the pockets; and

(e) forming a conductive material over the dielectric material and within at least some of the plurality of pockets.

108. (New) The method of claim 107, further comprising forming a plurality of vias extending through the insert substrate to the second side which are in electrical communication with at least some of the plurality of pockets.

109. (New) The method of claim 108, further comprising forming a plurality of conductive projections at the second side in electrical communication with at least some of the plurality of vias, the conductive projections receivable by at least some of the plurality of conductive members.

110. (New) The method of claim 109, wherein the conductive projections are formed by:

(a) forming a stencil on the second side, the stencil containing holes at the vicinity of the vias;

(b) filing the holes with a conductive substance; and

(c) removing the stencil.

111. (New) The method of claim 110, wherein the holes are filed with a melted conductive substance.

112. (New) The method of claim 111, further comprising drawing a blade across a surface of the stencil to remove excess melted conductive substance from the stencil surface.

113. (New) The method of claim 110, further comprising heating the conductive substance to form a bump.

114. (New) The method of claim 107, wherein the insert substrate comprises a monocrystal.

115. (New) The method of claim 114, wherein the monocrystal comprises silicon.

116. (New) The method of claim 107, wherein the recess is formed to receive the protrusion with clearance when the contact bumps are received in the plurality of pockets.

117. (New) The method of claim 107, wherein the pockets and the recess are formed to substantially the same depth.

118. (New) The method of claim 117, wherein the pockets and the recess are formed simultaneously.

119. (New) The method of claim 107, wherein the conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

120. (New) The method of claim 109, further comprising forming a dielectric material between (i) the via and the insert substrate, and (ii) the conductive projections and the insert substrate.

121. (New) The method of claim 120, wherein the dielectric material is silicon dioxide.

122. (New) The method of claim 107, wherein the pockets are formed with walls sloped at an angle of about 40-70 degrees relative a plane defined by said substrate.

123. (New) The method of claim 109, wherein the conductive projections comprise solder and are capable of being melted and adhered to the conductive members.

124. (New) The method of claim 109, wherein the conductive projections are bumps.

125. (New) The method of claim 107, wherein the pockets and the recess are formed using a wet etchant.

126. (New) The method of claim 120, wherein the wet etchant comprises potassium hydroxide.

127. (New) A method for making an insert for electrically interfacing an electronic device to a support substrate, the electronic device containing a plurality of contact bumps and a protrusion, the support substrate containing a plurality of conductive members, the insert having first and second sides, the method comprising:

(a) providing an insert substrate;

(b) forming in the first side of the insert substrate a plurality of pockets configured to receive and contact the contact bumps;

(c) forming a plurality of vias through the insert substrate to the second side which are in electrical communication with at least some of the plurality of pockets;

(d) forming a stencil on the second side of the insert substrate, the stencil containing holes at the vicinity of the vias;

(e) filing the holes with a conductive substance; and

(f) removing the stencil to form conductive projections in electrical communication with the vias and receivable by the conductive members.

128. (New) The method of claim 127, wherein forming the vias involves the use of a laser.

129. (New) The method of claim 127, wherein the holes are filed with a melted conductive substance.

130. (New) The method of claim 129, further comprising drawing a blade across a surface of the stencil to remove excess melted conductive substance from the stencil surface.

131. (New) The method of claim 127, further comprising heating the conductive projections to form a bump.

132. (New) The method of claim 127, wherein the insert substrate comprises a monocrystal.

133. (New) The method of claim 132, wherein the monocrystal comprises silicon.

134. (New) The method of claim 127, further comprising forming in the first side of the insert substrate a recess configured to receive the protrusion when the contact bumps are received in the plurality of pockets.

135. (New) The method of claim 134, wherein the recess is formed to receive the protrusion with clearance when the contact bumps are received in the plurality of pockets.

136. (New) The method of claim 134, wherein the pockets and the recess are formed to substantially the same depth.

137. (New) The method of claim 134, wherein the pockets and the recess are formed simultaneously.

138. (New) The method of claim 127, further comprising forming a dielectric material in the plurality of pockets.

139. (New) The method of claim 138, further comprising forming a dielectric material between (i) the via and the insert substrate, and (ii) the conductive projections and the insert substrate.

140. (New) The method of claim 138, further comprising forming a conductive material over the dielectric material and within at least some of the plurality of pockets.

141. (New) The method of claim 140, wherein the conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

142. (New) The method of claim 138, wherein the dielectric material is silicon dioxide.

143. (New) The method of claim 127, wherein the pockets are formed with walls sloped at an angle of about 40-70 degrees relative a plane defined by said substrate.

144. (New) The method of claim 127, wherein the conductive projections comprise solder and are capable of being melted and adhered to the conductive members.

145. (New) The method of claim 109, wherein the conductive projections are bumps.

146. (New) The method of claim 134, wherein the pockets and the recess are formed using a wet etchant.

147. (New) The method of claim 146, wherein the wet etchant comprises potassium hydroxide.

• **Please amend the specification as follows:**

(1) Please change the Title of the Specification to "Method of Forming A Test Insert For Interfacing A Device Containing Contact Bumps With A Test Substrate."

(2) Please add after the title of the specification: "This application is a divisional of co-pending application serial no. 09/250,994, filed February 16, 1999, to which priority is claimed."

(3) Please delete the paragraph beginning at page 2, line 3, and replace with the following paragraph:

--Recent trends of the semiconductor industry have led to development of smaller size semiconductor die. At the same time, the number of input/output lines required for the die have remained the same or have increased, thereby increasing their input/output densities. To accommodate these input/output density enhancements, the semiconductor [manufactures] manufacturers have developed alternative chip-scale packages.--

(4) Please delete the paragraph beginning at page 2, line 23, and replace with the following paragraph:

--Prior art, BGA test inserts, for example the insert as shown in Fig. 1, may not provide reliable testing of the globbed chip-scale-packaged, microelectronic devices. When using such prior art, test insert to test globbed chip-scale-packaged, microelectronic devices, a region of upper surface 19 of the test insert may contact the encapsulant protrusion 36 of the globbed chip-scale-packaged microelectronic device, so as to [interfer] interfere and prevent engagement of its outwardly projecting-contacts 14 with respective pockets 16 of the test insert 10.--

(5) Please delete the paragraph beginning at page 3, line 29, and replace with the following paragraph:

--These and other features of the present invention will become more fully apparent in the following description and independent claims, or [maybe] may be learned by the practice of the invention as set forth hereinafter.--

(6) Please delete the paragraph beginning at page 4, line 2, and replace with the following paragraph:

--The present invention will be understood from reading the following description of the particular embodiments with reference to specific embodiments illustrated in the intended drawings. Understanding that these drawings depict only particular embodiments of the invention and are not therefore to be considered limiting of its scope, the invention will be described and explained with [addition] additional detail through use of the accompanying drawings in which:--

(7) Please delete the paragraph beginning at page 6, line 13, and replace with the following paragraph:

--The present invention relates to formation of an insert for receiving and testing a "globbed" chip-scale-packaged microelectronic device having an array of outwardly projecting

contacts, e.g., of a ball-grid-array or bump-grid-array (BGA). Such insert may also be known by other terms such as, for [exemple] example, interconnect, interposer, socket, BGA test socket, or silicon insert.--

(8) Please delete the paragraph beginning at page 7, line 1, and replace with the following paragraph:

--Recent trends of the semiconductor industry have reduced semiconductor die size, while increasing the number of input/output interconnects. These changes have lead to development of newer ball-grid-array or bump-grid-array (i.e., BGA) interface solutions [cpable] capable of accommodating the smaller die of increased I/O densities. One such exemplary, prior art, BGA interface package comprises the globbed chip-scale-package.--

(9) Please delete the paragraph beginning at page 7, line 26, and replace with the following paragraph:

--Continuing with reference to Figs. 3A-3C, when trying to seat such globbed chip-scale-packaged microelectronic device 38 over prior art BGA test inserts – i.e., an insert similar to that of Fig. 1 – the encapsulant projection 36 of the package may confront a region of the upper surface of the insert [to] as to interfere with and prevent the outwardly projecting contacts 14 of the device from engaging respective pockets 16 of the prior art insert.--

(10) Please delete the paragraph beginning at page 9, line 20, and replace with the following paragraph:

--After [the] etching the pockets 16 and recess 17, mask 42 is removed and a dielectric 22 – for example, an oxide, nitride, carbide or the like – formed conformably over substrate 40, see Fig. 11. Dielectric 22 is formed by a known deposition process such as, for example, chemical vapor deposition (CVD).--

(11) Please delete the paragraph beginning at page 10, line 9, and replace with the following paragraph:

--Conductive layer 20 may comprise material of group IIIB through VIIIB metals, such as (but not limited to) the refractory metals, e.g., aluminum, iridium, copper, titanium, tungsten, tantalum, molybdenum, or alloys thereof. Conductive layer 20 might alternatively comprise other electrically conductive material such as, for example, metal-nitride of titanium-nitride or a silicide such as titanium-silicide. In a preferred exemplary embodiment, conductive layer 20, at regions associated with pockets 16, comprises an upper layer of titanium over a lower layer of aluminum. The upper layer is selected to prevent permanent or chemical bonding of the pocket liners to the conductive material of the outwardly projecting contacts to be seated therein. These conductive materials may be formed using known metal deposition processes, e.g., sputter, CVD, or PVD deposition. Additionally, the conductive materials can be patterned using known photolithographic, masking and etch procedures.--

(12) Please delete the paragraph beginning at page 10, line 20, and replace with the following paragraph:

--In another exemplary embodiment, conductive layer 20, at regions associated with bond pads 21, comprises a stack of two different layers, e.g., a lower barrier layer and an upper bonding layer to which wire bonds may be attached, as set forth in U.S. Patent Number 5,592,736, issued January 14, 1997, entitled "Fabricating An Interconnect For Testing Unpackaged Semiconductor Dice Having Raised Bond Pads", which is hereby incorporated by reference. See also U.S. Patent [application Serial Number 09/110,554 filed July 6, 1998, entitled "Metalized Recess In A Substrate And Method Of Making The Same"] Number 6,248,429, issued June 19, 2001, entitled "Metallized Recess In A Substrate", which is also incorporated herein by reference. In particular, the barrier and bonding layers are formulated to prevent oxidation of conductive materials associated with the interconnects, which oxidation might otherwise change the resistance of its contacts. The bonding layer is selected to facilitate wire bonding thereto. In a preferred exemplary embodiment, the barrier layer comprises a metal

such as platinum, titanium, tungsten, or alloys thereof. As patterned, certain portions of conductive layer 20 define traces 23 while other portions define bond pad 21 in electrical communication with the conductive liners of pockets 16. Methods of forming the conductive material, traces and liners can be found in U.S. Patent [Application Serial Number 09/110,554, filed July 6, 1998, entitled "Metalized Recess In A Substrate And Method Of Making The Same"] Number 6,248,429, issued June 19, 2001, entitled "Metallized Recess In A Substrate", again incorporated herein by reference. In other more specific exemplary embodiments, regions of the conductive layer 20 associated with the bond pads may comprise multiple layers of conductive material such as, for example, a four layer stack (not shown) comprising titanium, tungsten, titanium and aluminum respectively.--

(13) Please delete the paragraph beginning at page 12, line 12, and replace with the following paragraph:

--In the illustrated exemplary embodiment, cover 54 acts together with biasing member 52 and force plate 50 to apply a biasing force against the globbed chip-scale-packaged microelectronic device 38, thereby forcibly engaging its outwardly projecting contacts 14 against pockets 16 of insert 10. Cover 54 includes clips 53 and tabs 57. Tabs 57, at the ends of clips 53, are received and captured by clamp ring 56 for securing the cover 54 to base 48. Cover 54 preferably comprises resilient metal, such as steel. Force plate 50 preferably comprises a solid material such as metal, plastic or ceramic. The force plate 50 is shaped to engage and apply a force across various surfaces of the globbed chip-scale-packaged microelectronic device 38. Biasing member 52 is disposed between the inside surface of cover 54 and force plate 50 to apply a force against force plate 50 when cover 54 is secured to base 48. Biasing member 52 preferably comprises a resilient elastomeric material – e.g., silicone, butyl rubber, flouorsilicone, and polyimide – capable of exerting a biasing force over a continued life span. Additional aspects concerning elements of test jig 59 and its assembly are provided by U.S. Patent Application Number 09/_____, filed _____, entitled "Test Carrier With Variable Force Applying Mechanism For Testing Semiconductor Components" (98-0333), and U.S. Patent

Number 5,796,264 entitled "Apparatus For Manufacturing Known Good Semiconductor Die", which application and patent are incorporated herein by reference.--

(14) Please delete the paragraph beginning at page 16, line 20, and replace with the following paragraph:

--Thus, the present invention provides a new insert, method for forming an insert and method of testing a globbed chip-scale-packaged microelectronic device. Although the foregoing invention has been described with respect to certain exemplary embodiments, other embodiments will become apparent in view of the disclosure herein. Accordingly, the described embodiments are to be considered only as illustrative and not restrictive. The scope of the invention, therefore, is indicated by the appended claims and [there] their combination in whole or in part rather than by the foregoing description. All changes thereto which come within the meaning and range of the equivalent of the claims are to be embraced within the scope of the claims.--

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II. REMARKS

Claims 1-106 have been deleted and new claims 107-147 added. A clean copy of all pending claims is attached for the examiner's convenience.

Certain typographical errors and other minor changes have been made to the specification, none of which add new matter. A copy of the paragraphs showing these edits, as well as clean copies of these paragraphs, are attached for the examiner's convenience.

In order to facilitate the resolution of any questions presented by this paper, Applicant invites the Examiner to directly contact the undersigned by phone (713-787-1499).

Respectfully submitted,

Terril G. Lewis, Esq.
Reg. No. 46,065
Tel. 713 787 1499
Date: July 27, 2001

Clean Copy of Pending Claims As Amended By This Response

107. A method for making an insert for electrically interfacing an electronic device to a support substrate, the electronic device containing a plurality of contact bumps and a protrusion, the support substrate containing a plurality of conductive members, the insert having first and second sides, the method comprising:

(a) providing an insert substrate;

(b) forming in the first side of the insert substrate a plurality of pockets configured to receive and contact the contact bumps;

(c) forming in the first side of the insert substrate a recess configured to receive the protrusion when the contact bumps are received in the plurality of pockets;

(d) forming a dielectric material over the pockets; and

(e) forming a conductive material over the dielectric material and within at least some of the plurality of pockets.

108. The method of claim 107, further comprising forming a plurality of vias extending through the insert substrate to the second side which are in electrical communication with at least some of the plurality of pockets.

109. The method of claim 108, further comprising forming a plurality of conductive projections at the second side in electrical communication with at least some of the plurality of vias, the conductive projections receivable by at least some of the plurality of conductive members.

110. The method of claim 109, wherein the conductive projections are formed by:

(a) forming a stencil on the second side, the stencil containing holes at the vicinity of the vias;

(b) filing the holes with a conductive substance; and

(c) removing the stencil.

111. The method of claim 110, wherein the holes are filed with a melted conductive substance.

112. The method of claim 111, further comprising drawing a blade across a surface of the stencil to remove excess melted conductive substance from the stencil surface.

113. The method of claim 110, further comprising heating the conductive substance to form a bump.

114. The method of claim 107, wherein the insert substrate comprises a monocrystal.

115. The method of claim 114, wherein the monocrystal comprises silicon.

116. The method of claim 107, wherein the recess is formed to receive the protrusion with clearance when the contact bumps are received in the plurality of pockets.

117. The method of claim 107, wherein the pockets and the recess are formed to substantially the same depth.

118. The method of claim 117, wherein the pockets and the recess are formed simultaneously.

119. The method of claim 107, wherein the conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

120. The method of claim 109, further comprising forming a dielectric material between (i) the via and the insert substrate, and (ii) the conductive projections and the insert substrate.

121. The method of claim 120, wherein the dielectric material is silicon dioxide.

122. The method of claim 107, wherein the pockets are formed with walls sloped at an angle of about 40-70 degrees relative a plane defined by said substrate.

123. The method of claim 109, wherein the conductive projections comprise solder and are capable of being melted and adhered to the conductive members.

124. The method of claim 109, wherein the conductive projections are bumps.

125. The method of claim 107, wherein the pockets and the recess are formed using a wet etchant.

126. The method of claim 120, wherein the wet etchant comprises potassium hydroxide.

127. A method for making an insert for electrically interfacing an electronic device to a support substrate, the electronic device containing a plurality of contact bumps and a protrusion, the support substrate containing a plurality of conductive members, the insert having first and second sides, the method comprising:

(a) providing an insert substrate;

(b) forming in the first side of the insert substrate a plurality of pockets configured to receive and contact the contact bumps;

(c) forming a plurality of vias through the insert substrate to the second side which are in electrical communication with at least some of the plurality of pockets;

(d) forming a stencil on the second side of the insert substrate, the stencil containing holes at the vicinity of the vias;

(e) filing the holes with a conductive substance; and

(f) removing the stencil to form conductive projections in electrical communication with the vias and receivable by the conductive members.

128. The method of claim 127, wherein forming the vias involves the use of a laser.

129. The method of claim 127, wherein the holes are filed with a melted conductive substance.

130. The method of claim 129, further comprising drawing a blade across a surface of the stencil to remove excess melted conductive substance from the stencil surface.

131. The method of claim 127, further comprising heating the conductive projections to form a bump.

132. The method of claim 127, wherein the insert substrate comprises a monocrystal.

133. The method of claim 132, wherein the monocrystal comprises silicon.

134. The method of claim 127, further comprising forming in the first side of the insert substrate a recess configured to receive the protrusion when the contact bumps are received in the plurality of pockets.

135. The method of claim 134, wherein the recess is formed to receive the protrusion with clearance when the contact bumps are received in the plurality of pockets.

136. The method of claim 134, wherein the pockets and the recess are formed to substantially the same depth.

137. The method of claim 134, wherein the pockets and the recess are formed simultaneously.

138. The method of claim 127, further comprising forming a dielectric material in the plurality of pockets.

139. The method of claim 138, further comprising forming a dielectric material between (i) the via and the insert substrate, and (ii) the conductive projections and the insert substrate.

140. The method of claim 138, further comprising forming a conductive material over the dielectric material and within at least some of the plurality of pockets.

141. The method of claim 140, wherein the conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

142. The method of claim 138, wherein the dielectric material is silicon dioxide.

143. The method of claim 127, wherein the pockets are formed with walls sloped at an angle of about 40-70 degrees relative a plane defined by said substrate.

144. The method of claim 127, wherein the conductive projections comprise solder and are capable of being melted and adhered to the conductive members.

145. The method of claim 109, wherein the conductive projections are bumps.

146. The method of claim 134, wherein the pockets and the recess are formed using a wet etchant.

147. The method of claim 146, wherein the wet etchant comprises potassium hydroxide.

Clean Copy of Specification Paragraphs As Amended By This Response

New Title:

Method of Forming A Test Insert For Interfacing A Device Containing Contact Bumps With A Test Substrate

After the Title:

This application is a divisional of co-pending application serial no. 09/250,994, filed February 16, 1999, to which priority is claimed

Page 2, line 3:

Recent trends of the semiconductor industry have led to development of smaller size semiconductor die. At the same time, the number of input/output lines required for the die have remained the same or have increased, thereby increasing their input/output densities. To accommodate these input/output density enhancements, the semiconductor manufacturers have developed alternative chip-scale packages.

Page 2, line 23:

Prior art, BGA test inserts, for example the insert as shown in Fig. 1, may not provide reliable testing of the globbed chip-scale-packaged, microelectronic devices. When using such prior art, test insert to test globbed chip-scale-packaged, microelectronic devices, a region of upper surface 19 of the test insert may contact the encapsulant protrusion 36 of the globbed chip-scale-packaged microelectronic device, so as to interfere and prevent engagement of its outwardly projecting-contacts 14 with respective pockets 16 of the test insert 10.

Page 3, line 29:

These and other features of the present invention will become more fully apparent in the following description and independent claims, or may be learned by the practice of the invention as set forth hereinafter.

Page 4, line 2:

The present invention will be understood from reading the following description of the particular embodiments with reference to specific embodiments illustrated in the intended drawings. Understanding that these drawings depict only particular embodiments of the invention and are not therefore to be considered limiting of its scope, the invention will be described and explained with additional detail through use of the accompanying drawings in which:

Page 6, line 13:

The present invention relates to formation of an insert for receiving and testing a "globbed" chip-scale-packaged microelectronic device having an array of outwardly projecting contacts, e.g., of a ball-grid-array or bump-grid-array (BGA). Such insert may also be known by other terms such as, for example, interconnect, interposer, socket, BGA test socket, or silicon insert.

Page 7, line 1:

Recent trends of the semiconductor industry have reduced semiconductor die size, while increasing the number of input/output interconnects. These changes have lead to development of newer ball-grid-array or bump-grid-array (i.e., BGA) interface solutions capable of accommodating the smaller die of increased I/O densities. One such exemplary, prior art, BGA interface package comprises the globbed chip-scale-package.

Page 7, line 26:

Continuing with reference to Figs. 3A-3C, when trying to seat such globbed chip-scale-packaged microelectronic device 38 over prior art BGA test inserts – i.e., an insert similar to that of Fig. 1 – the encapsulant projection 36 of the package may confront a region of the upper surface of the insert as to interfere with and prevent the outwardly projecting contacts 14 of the device from engaging respective pockets 16 of the prior art insert.

Page 9, line 20:

After etching the pockets 16 and recess 17, mask 42 is removed and a dielectric 22 – for example, an oxide, nitride, carbide or the like – formed conformably over substrate 40, see Fig. 11. Dielectric 22 is formed by a known deposition process such as, for example, chemical vapor deposition (CVD).

Page 10, line 9:

Conductive layer 20 may comprise material of group IIIB through VIIIB metals, such as (but not limited to) the refractory metals, e.g., aluminum, iridium, copper, titanium, tungsten, tantalum, molybdenum, or alloys thereof. Conductive layer 20 might alternatively comprise other electrically conductive material such as, for example, metal-nitride of titanium-nitride or a silicide such as titanium-silicide. In a preferred exemplary embodiment, conductive layer 20, at regions associated with pockets 16, comprises an upper layer of titanium over a lower layer of aluminum. The upper layer is selected to prevent permanent or chemical bonding of the pocket liners to the conductive material of the outwardly projecting contacts to be seated therein. These conductive materials may be formed using known metal deposition processes, e.g., sputter, CVD, or PVD deposition. Additionally, the conductive materials can be patterned using known photolithographic, masking and etch procedures.

Page 10, line 20:

In another exemplary embodiment, conductive layer 20, at regions associated with bond pads 21, comprises a stack of two different layers, e.g., a lower barrier layer and an upper

bonding layer to which wire bonds may be attached, as set forth in U.S. Patent Number 5,592,736, issued January 14, 1997, entitled "Fabricating An Interconnect For Testing Unpackaged Semiconductor Dice Having Raised Bond Pads", which is hereby incorporated by reference. See also U.S. Patent Number 6,248,429, issued June 19, 2001, entitled "Metallized Recess In A Substrate", which is also incorporated herein by reference. In particular, the barrier and bonding layers are formulated to prevent oxidation of conductive materials associated with the interconnects, which oxidation might otherwise change the resistance of its contacts. The bonding layer is selected to facilitate wire bonding thereto. In a preferred exemplary embodiment, the barrier layer comprises a metal such as platinum, titanium, tungsten, or alloys thereof. As patterned, certain portions of conductive layer 20 define traces 23 while other portions define bond pad 21 in electrical communication with the conductive liners of pockets 16. Methods of forming the conductive material, traces and liners can be found in U.S. Patent Number 6,248,429, issued June 19, 2001, entitled "Metallized Recess In A Substrate", again incorporated herein by reference. In other more specific exemplary embodiments, regions of the conductive layer 20 associated with the bond pads may comprise multiple layers of conductive material such as, for example, a four layer stack (not shown) comprising titanium, tungsten, titanium and aluminum respectively.

Page 12, line 12:

In the illustrated exemplary embodiment, cover 54 acts together with biasing member 52 and force plate 50 to apply a biasing force against the globbed chip-scale-packaged microelectronic device 38, thereby forcibly engaging its outwardly projecting contacts 14 against pockets 16 of insert 10. Cover 54 includes clips 53 and tabs 57. Tabs 57, at the ends of clips 53, are received and captured by clamp ring 56 for securing the cover 54 to base 48. Cover 54 preferably comprises resilient metal, such as steel. Force plate 50 preferably comprises a solid material such as metal, plastic or ceramic. The force plate 50 is shaped to engage and apply a force across various surfaces of the globbed chip-scale-packaged microelectronic device 38. Biasing member 52 is disposed between the inside surface of cover 54 and force plate 50 to

apply a force against force plate 50 when cover 54 is secured to base 48. Biasing member 52 preferably comprises a resilient elastomeric material – e.g., silicone, butyl rubber, flouorsilicone, and polyimide – capable of exerting a biasing force over a continued life span. Additional aspects concerning elements of test jig 59 and its assembly are provided by U.S. Patent Application Number 09/_____, filed _____, entitled "Test Carrier With Variable Force Applying Mechanism For Testing Semiconductor Components" (98-0333), and U.S. Patent Number 5,796,264 entitled "Apparatus For Manufacturing Known Good Semiconductor Die", which application and patent are incorporated herein by reference.

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Thus, the present invention provides a new insert, method for forming an insert and method of testing a globbed chip-scale-packaged microelectronic device. Although the foregoing invention has been described with respect to certain exemplary embodiments, other embodiments will become apparent in view of the disclosure herein. Accordingly, the described embodiments are to be considered only as illustrative and not restrictive. The scope of the invention, therefore, is indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes thereto which come within the meaning and range of the equivalent of the claims are to be embraced within the scope of the claims.

Copy of Specification Paragraphs Showing Amendments

Title:

[Insert For Testing A Microelectronic Device Having A Plurality Of Raised-Contacts And Method Of Making The Same] Method of Forming A Test Insert For Interfacing A Device Containing Contact Bumps With A Test Substrate

After the Title:

This application is a divisional of co-pending application serial no. 09/250,994, filed February 16, 1999, to which priority is claimed.

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These and other features of the present invention will become more fully apparent in the following description and independent claims, or [maybe] may be learned by the practice of the invention as set forth hereinafter.

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The present invention relates to formation of an insert for receiving and testing a "globbed" chip-scale-packaged microelectronic device having an array of outwardly projecting contacts, e.g., of a ball-grid-array or bump-grid-array (BGA). Such insert may also be known by other terms such as, for [exemple] example, interconnect, interposer, socket, BGA test socket, or silicon insert.

Page 7, line 1:

Recent trends of the semiconductor industry have reduced semiconductor die size, while increasing the number of input/output interconnects. These changes have lead to development of newer ball-grid-array or bump-grid-array (i.e., BGA) interface solutions [cpable] capable of accommodating the smaller die of increased I/O densities. One such exemplary, prior art, BGA interface package comprises the globbed chip-scale-package.

Page 7, line 26:

Continuing with reference to Figs. 3A-3C, when trying to seat such globbed chip-scale-packaged microelectronic device 38 over prior art BGA test inserts – i.e., an insert similar to that of Fig. 1 – the encapsulant projection 36 of the package may confront a region of the upper surface of the insert [to] as to interfere with and prevent the outwardly projecting contacts 14 of the device from engaging respective pockets 16 of the prior art insert.

Page 9, line 20:

After [the] etching the pockets 16 and recess 17, mask 42 is removed and a dielectric 22 – for example, an oxide, nitride, carbide or the like – formed conformably over substrate 40, see Fig. 11. Dielectric 22 is formed by a known deposition process such as, for example, chemical vapor deposition (CVD).

Page 10, line 9:

Conductive layer 20 may comprise material of group IIIB through VIIIB metals, such as (but not limited to) the refractory metals, e.g., aluminum, iridium, copper, titanium, tungsten, tantalum, molybdenum, or alloys thereof. Conductive layer 20 might alternatively comprise other electrically conductive material such as, for example, metal-nitride of titanium-nitride or a silicide such as titanium-silicide. In a preferred exemplary embodiment, conductive layer 20, at regions associated with pockets 16, comprises an upper layer of titanium over a lower layer of aluminum. The upper layer is selected to prevent permanent or chemical bonding of the pocket liners to the conductive material of the outwardly projecting contacts to be seated therein. These conductive materials may be formed using known metal deposition processes, e.g., sputter, CVD, or PVD deposition. Additionally, the conductive materials can be patterned using known photolithographic, masking and etch procedures.

Page 10, line 20:

In another exemplary embodiment, conductive layer 20, at regions associated with bond pads 21, comprises a stack of two different layers, e.g., a lower barrier layer and an upper

bonding layer to which wire bonds may be attached, as set forth in U.S. Patent Number 5,592,736, issued January 14, 1997, entitled "Fabricating An Interconnect For Testing Unpackaged Semiconductor Dice Having Raised Bond Pads", which is hereby incorporated by reference. See also U.S. Patent [application Serial Number 09/110,554 filed July 6, 1998, entitled "Metalized Recess In A Substrate And Method Of Making The Same"] Number 6,248,429, issued June 19, 2001, entitled "Metallized Recess In A Substrate", which is also incorporated herein by reference. In particular, the barrier and bonding layers are formulated to prevent oxidation of conductive materials associated with the interconnects, which oxidation might otherwise change the resistance of its contacts. The bonding layer is selected to facilitate wire bonding thereto. In a preferred exemplary embodiment, the barrier layer comprises a metal such as platinum, titanium, tungsten, or alloys thereof. As patterned, certain portions of conductive layer 20 define traces 23 while other portions define bond pad 21 in electrical communication with the conductive liners of pockets 16. Methods of forming the conductive material, traces and liners can be found in U.S. Patent [Application Serial Number 09/110,554, filed July 6, 1998, entitled "Metalized Recess In A Substrate And Method Of Making The Same"] Number 6,248,429, issued June 19, 2001, entitled "Metallized Recess In A Substrate", again incorporated herein by reference. In other more specific exemplary embodiments, regions of the conductive layer 20 associated with the bond pads may comprise multiple layers of conductive material such as, for example, a four layer stack (not shown) comprising titanium, tungsten, titanium and aluminum respectively.

Page 12, line 12:

In the illustrated exemplary embodiment, cover 54 acts together with biasing member 52 and force plate 50 to apply a biasing force against the globbed chip-scale-packaged microelectronic device 38, thereby forcibly engaging its outwardly projecting contacts 14 against pockets 16 of insert 10. Cover 54 includes clips 53 and tabs 57. Tabs 57, at the ends of clips 53, are received and captured by clamp ring 56 for securing the cover 54 to base 48. Cover 54 preferably comprises resilient metal, such as steel. Force plate 50 preferably comprises a solid

material such as metal, plastic or ceramic. The force plate 50 is shaped to engage and apply a force across various surfaces of the globbed chip-scale-packaged microelectronic device 38. Biasing member 52 is disposed between the inside surface of cover 54 and force plate 50 to apply a force against force plate 50 when cover 54 is secured to base 48. Biasing member 52 preferably comprises a resilient elastomeric material – e.g., silicone, butyl rubber, flouorsilicone, and polyimide – capable of exerting a biasing force over a continued life span. Additional aspects concerning elements of test jig 59 and its assembly are provided by U.S. Patent Application Number 09/_____, filed _____, entitled "Test Carrier With Variable Force Applying Mechanism For Testing Semiconductor Components" (98-0333), and U.S. Patent Number 5,796,264 entitled "Apparatus For Manufacturing Known Good Semiconductor Die", which application and patent are incorporated herein by reference.

Page 16, line 20:

Thus, the present invention provides a new insert, method for forming an insert and method of testing a globbed chip-scale-packaged microelectronic device. Although the foregoing invention has been described with respect to certain exemplary embodiments, other embodiments will become apparent in view of the disclosure herein. Accordingly, the described embodiments are to be considered only as illustrative and not restrictive. The scope of the invention, therefore, is indicated by the appended claims and [there] their combination in whole or in part rather than by the foregoing description. All changes thereto which come within the meaning and range of the equivalent of the claims are to be embraced within the scope of the claims.